

**CLAIMS**

Now, therefore, the following is claimed:

- 1           1.       A computer system for processing instructions of a computer program,  
2       comprising:  
3           a plurality of pipelines configured to process and execute said instructions; and  
4           a scoreboard coupled to said pipeline, said scoreboard having a plurality of  
5       multi-bit registers, said scoreboard configured to receive a register identifier from one  
6       of said pipelines and to change a first bit in one of said multi-bit registers in response  
7       to said register identifier, said first bit indicating whether a pending write to a register  
8       identified by said register identifier exists, said register identifier associated with one  
9       of said instructions processed by said pipeline, said scoreboard further configured to  
10      receive data associated with said one instruction and to change a second bit in said one  
11      register based on said received data.
- 1           2,       The system of claim 1, wherein said data associated with said one  
2       instruction includes a speculative bit.
- 1           3.       The system of claim 1, wherein said one instruction is a load  
2       instruction and said data associated with said one instruction is indicative of which  
3       memory locations have been searched in response to said one instruction.
- 1           4.       The system of claim 3, further comprising circuitry configured to detect  
2       whether said one instruction can be canceled based on said second bit.

1           5.       The system of claim 1, further comprising circuitry coupled to said  
2 scoreboard, said circuitry configured to detect a data hazard based on said first and  
3 second bits.

1           6.       The system of claim 5, wherein said second bit indicates whether said  
2 one instruction is speculative, said circuitry further configured to detect whether  
3 another instruction being processed by one of said pipelines utilizes said register  
4 identified by said register identifier and to modify said second bit in response to said  
5 other instruction.

1           7.       The system of claim 5, wherein said circuitry is further configured to  
2 modify said second bit.

1           8.     A method for processing instructions of a computer program,  
2     comprising the steps of:  
3           providing a pipeline and a scoreboard, said scoreboard including a plurality of  
4     multi-bit registers;  
5           processing one of said instructions via said pipeline;  
6           transmitting a register identifier defined by said one instruction to said  
7     scoreboard;  
8           changing a first bit in one of said multi-bit registers based on said register  
9     identifier;  
10          transmitting data associated with said one instruction to said scoreboard;  
11          changing a second bit in said one register based on said data; and  
12          detecting that data produced via execution of said one instruction is  
13     unavailable; and  
14          performing said changing a first bit step in response to said step of detecting  
15     that data produced via execution of said one instruction is unavailable.

1           9.     The method of claim 8, further comprising the step of detecting a data  
2     hazard based on said first and second bits.

1           10.    The method of claim 8, further comprising the step of indicating, via  
2     said second bit, a speculative state of said one instruction.

1           11.     The method of claim 8, further comprising the steps of:  
2           detecting whether another instruction, when executed, utilizes a register  
3           identified by said register identifier; and  
4           changing said second bit based on said detecting whether another instruction  
5           utilizes said register step.

1           12.     The method of claim 8, further comprising the steps of:  
2           retiring said one instruction; and  
3           performing said changing a first bit step in response to said retiring step.

1           13.     The method of claim 8, wherein said processing step further includes  
2           the step of executing said one instruction and said method further includes the steps  
3           of:  
4           receiving data produced in response to said executing step; and  
5           changing said first bit in response to said receiving step.

1           14.     The method of claim 8, further comprising the steps of:  
2           retrieving data in response to said one instruction; and  
3           indicating, via said second bit, how far said retrieving step has progressed.

1           15.     The method of claim 14, further comprising the steps of:  
2           detecting whether said one instruction can be canceled based on said second  
3           bit; and  
4           canceling said one instruction based on said detecting whether said one  
5           instruction can be canceled step.

1           16.     The method of claim 8, further comprising the steps of:  
2           selecting said one register based on said register identifier; and  
3           performing said changing a first bit step in response to said selecting step.

1           17.     The method of claim 16, further comprising the step of:  
2           performing said changing a second bit step in response to said selecting step.

1           18.     A method for processing instructions of a computer program,  
2     comprising the steps of:  
3           providing at least one pipeline and a scoreboard, said scoreboard including at  
4     least one multi-bit register;  
5           processing at least one instruction via said one pipeline;  
6           identifying a register based on a register identifier defined by said one  
7     instruction;  
8           detecting whether data produced via execution of said one instruction has been  
9     written to said register identified in said identifying step;  
10          transmitting said register identifier to said scoreboard in response to a  
11     detection in said detecting step that said data produced via execution of said one  
12     instruction has yet to be written to said register identified in said identifying step;  
13          changing a first bit in said one register based on said register identifier  
14     transmitted in said transmitting said register identifier step;  
15          receiving, at said scoreboard, data associated with said one instruction;  
16          changing a second bit in said one register based on said data received in said  
17     receiving step; and

18           detecting a data hazard based on said first and second bits.

1           19.     The method of claim 18, further comprising the steps of:

2           retiring said one instruction; and

3           performing said changing a first bit step in response to said retiring step.